

**IN THE CLAIMS:**

Please cancel claims 7-10 and 28-31. Please also amend claims 1, 12-15, and 20-22, and add new claims 32-34, so that a complete set of the pending claims will read as follows:

1. (Currently Amended) A method for accessing initialization data for starting up a central processor unit in a computer system comprising:
  - (a) starting up a north-bridge chip that is ~~connected~~ coupled between the central processor unit and ~~a bus~~ a south-bridge chip;
  - (b) sending a request ~~for said initialization data~~ from said north-bridge chip to ~~[[a]]~~ the south-bridge chip that is connected to the bus and in order to access the initialization data from a non-volatile memory which stores a basic input/output system (BIOS) and the initialization data;  
and
  - (c) upon receiving said initialization data from the south-bridge chip by said north-bridge chip, starting up the central processor unit for initialization of the central processor unit based on the received initialization data.
2. (Previously Presented) The method according to Claim 1 wherein said initialization data is serial initialization packet ("SIP") data of the central processor unit.
3. (Previously Presented) The method according to Claim 2 wherein said initialization data is SIP data for an AMD K7 processor.
4. (Previously Presented) The method according to Claim 1 wherein step (a) comprises starting up the north-bridge chip by said south-bridge chip.
5. (Previously Presented) The method according to Claim 1 wherein step (b) comprises sending a signal from said north-bridge chip to said south-bridge chip for requesting said initialization data.

6. (Previously Presented) The method according to Claim 1 further comprising sending said initialization data from said north-bridge chip to the central processor unit of said computer system for starting up the central processor unit.

7-11. (Cancelled)

12. (Currently Amended) A method for accessing initialization data for starting up a central processor unit in a computer system that also includes a bus, a south-bridge chip connected to the bus, a non-volatile memory ~~that stores the initialization data~~, and a north-bridge chip connected between the bus and the central processor unit, the method comprising:

(a) sending a request ~~for the initialization data~~ from the north-bridge chip to the south-bridge chip in order to access initialization data from the non-volatile memory, which stores a basic input/output system (BIOS) and the initialization data;

(b) in response to the request, using the south-bridge chip to accessing the non-volatile memory ~~[[and]]~~ to read out the initialization data by the south-bridge chip;

(c) sending the initialization data from the south-bridge chip to the north-bridge chip; and

(d) upon receiving the initialization data sent from the south-bridge chip, activating the central processor unit for initialization of the central processor unit based on the initialization data received by the north-bridge chip from the south-bridge chip.

13. (Currently Amended) The method of claim 12 further comprising activating the north-bridge chip by sending an initiating signal from the south-bridge chip to the north-bridge chip before step (a) is conducted.

14. (Currently Amended) The method of claim 13, further comprising activating the south-bridge chip by a power ~~supplier~~ supply before sending an initiating signal from the south-bridge chip to actuate the north-bridge chip.

15. (Currently Amended) The method of claim 12 wherein the non-volatile memory is a read only memory ~~containing a BIOS~~.

16. (Previously Presented) The method of claim 12 wherein the request sent in step (a) is a transaction sent from the north-bridge chip to the south-bridge chip requesting the south-bridge chip to retrieve the initialization data from the non-volatile memory.

17. (Previously Presented) The method of claim 12 wherein step (d) includes:  
receiving the initialization data by the north-bridge chip; and  
sending an initializing signal and the received initialization data to the central processor unit.

18. (Previously Presented) The method of claim 17 wherein the initialization data includes an initialization ID.

19. (Previously Presented) The method of claim 17 wherein the initialization data includes serial initialization packet ("SIP") data.

20. (Currently Amended) A system for accessing initialization data for starting a central processor unit, the system comprising:

~~a south-bridge chip;~~

~~a north-bridge chip in direct communication with the south-bridge chip and the central processor unit; and~~

~~a non-volatile memory subsystem in direct communication with the south-bridge chip storing a basic input/output system (BIOS) and the initialization data;~~

a south-bridge chip in direct communication with the non-volatile memory, the south-bridge chip, when requested for the initialization data, for accessing the initialization data from the non-volatile memory;

a north-bridge chip, coupled between the south-bridge chip and the central processor unit,  
the north-bridge chip, when activated, sending a request for the initialization data to the south-  
bridge chip;

wherein upon receiving ~~[[a]]~~ the request from the north-bridge chip for obtaining the  
initialization data, ~~the initialization data is accessed by the south-bridge chip~~ accesses the  
initialization data and ~~forwarded~~ forwards the initialization data to the north-bridge chip for  
activating the central processor unit;

wherein upon receiving the initialization data sent from the south-bridge chip, the north-  
bridge chip activates the central processor unit for initialization of the central processor unit  
based on the received initialization data from the south-bridge chip.

21. (Currently Amended) The system of claim 20 further comprising a power ~~supplier~~ supply  
for activating the south-bridge chip, wherein the south-bridge chip activates the north-bridge chip  
when the south-bridge chip is activated.

22. (Currently Amended) The system of claim 20 wherein the non-volatile memory is a read  
only memory ~~containing a BIOS.~~

23. (Original) The system of claim 22 wherein the non-volatile memory includes a  
predetermined location for storing the initialization data that is not occupied by the BIOS.

24. (Previously Presented) The system of claim 20 wherein the initialization data includes an  
initialization ID.

25. (Previously Presented) The system of claim 20 wherein the initialization data includes  
session initialization protocol data.

26. (Previously Presented) The system of claim 20 wherein the south-bridge chip includes  
means for:

activating the north-bridge chip;

retrieving the initialization data by the south-bridge chip; and  
sending the initialization data to the north-bridge chip.

27. (Previously Presented) The system of claim 20 where in the north-bridge chip further includes means for sending an initializing signal to the central processor unit based on the forwarded initialization data.

28-31. (Cancelled)

32. (New) The method of claim 1, wherein step (c) comprises:

upon receiving said initialization data from the south-bridge chip by said north-bridge chip, starting up the central processor unit to set initial values for initialization of the central processor unit based on the received initialization data.

33. (New) The method of claim 12, wherein step (d) comprises:

upon receiving the initialization data sent from the south-bridge chip, activating the central processor unit for to set initial values for initialization of the central processor unit based on the received initialization data received by the north-bridge chip from the south-bridge chip.

34. (New) The apparatus according to claim 20, wherein upon receiving the initialization data sent from the south-bridge, the north-bridge chip activates the central processor unit to set initial values for initialization of the central processor unit based on the received initialization data from the south-bridge chip.